

PATENT  
PD-10018774-1

METHOD OF FORMING ONE OR MORE NANOPORES FOR  
ALIGNING MOLECULES FOR MOLECULAR ELECTRONICS

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5        METHOD OF FORMING ONE OR MORE NANOPORES FOR  
ALIGNING MOLECULES FOR MOLECULAR ELECTRONICS10        STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH  
                 OR DEVELOPMENT

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13 terms as provided for by the terms of Contract No. MDA 97201-3-0005 awarded by the  
14 Defense Advanced Research Projects Agency.

15        TECHNICAL FIELD

16 [0002]        The present invention is related generally to forming nanopores useful  
17 for aligning molecules.

20        BACKGROUND ART

21 [0003]        The field of molecular electronics relies on ordered placement of mole-  
22 cules on a supporting substrate, which is often an electrode of an electronic device.  
23 For most applications, the molecules should have a definite orientation or be oriented  
24 with respect to the substrate plane, often perpendicular to it. Molecular films are often  
25 formed by Langmuir-Blodgett techniques to obtain a uniform monolayer or multi-  
26 layer film. However, the orientation of the molecules is often difficult to control using  
27 Langmuir-Blodgett techniques until carefully refined for each combination of mole-  
28 cule and substrate and even then may be complicated by domains. A more robust

method of aligning the molecules is needed using a technique that is less sensitive to the particular molecule being used. In addition, some applications require molecules to be spaced (separated) from each other; this cannot be readily accomplished by Langmuir-Blodgett techniques.

- 5    **[0004]**       One approach to providing spaced holes in a substrate (silicon nitride-coated silicon) is disclosed by M. Park et al, "Block Copolymer Lithography: Periodic Arrays of  $\sim 10^{11}$  Holes in 1 Square Centimeter", Science, Vol. 276, pp. 1401-1404 (30 May 1997). However, the block copolymer mask is easily ablated during reactive ion etching, thus limiting this approach in the depth of the holes that can be formed. Further, the block copolymers that are used are not commercially available, and must be synthesized for each use, which is inconvenient for use outside the laboratory.

#### DISCLOSURE OF INVENTION

- 15   **[0005]**       In accordance with the present invention, a method is provided for forming one molecule or an array of molecules aligned at a defined orientation to the substrate. The method is also useful for forming a mold for deposition of other materials therein and for spacing or separating molecules.

- 20   **[0006]**       The array of molecules is formed by dispersing them in a small single hole (nanopore) or in an array of small, aligned holes (nanopores) in a substrate. Typically, the material in which the pores are formed is electrically insulating. The underlying substrate may be either electrically conducting or insulating. For electronic device applications, the substrate is, in general, electrically conducting and may be exposed and accessible at the bottom of the pores so that one end of the molecule in the nanopore makes electrical contact to the substrate.

25   **[0007]**       The method for forming a nanopore array for aligning molecules for molecular electronic devices comprises:

30   **[0008]**       (a) providing a substrate having a first major surface and a second major surface, substantially parallel to the first major surface;

**[0009]**       (b) forming an etch mask on the first major surface, the etch mask comprising one or a plurality of nanoparticles;

[0010] (c) directionally etching the substrate from the first major surface toward the second major surface, using the etch mask to protect underlying portions of the substrate against the etching, thereby forming a plurality of pillars underneath the etch mask;

5 [0011] (d) forming a layer of insulating material on the surface of the etched substrate, including between the pillars and either partially covering or embedding the pillars; and

[0012] (e) removing the pillars to leave a plurality of nanopores in the insulating layer.

10 [0013] If the pillars are embedded, then between steps (d) and (e), a process step is added to expose the ends of the pillars.

[0014] During the directional etching, the substrate may be maintained normal to the etching source to thereby provide nanopores that are substantially perpendicular to the substrate. Alternatively, the substrate and the etching source may be maintained  
15 at a pre-selected angle relative to each other to provide nanopores that are in a defined orientation relative to the substrate.

[0015] The method of the present invention aligns the molecules in a fixed direction, using a technique that is less sensitive to the particular molecule being used.

20 BRIEF DESCRIPTION OF THE DRAWINGS

[0016] FIGS. 1a-1f are cross-sectional views, illustrating the method steps according to an embodiment of the present invention.

25 BEST MODES FOR CARRYING OUT THE INVENTION

[0017] The discussion which follows is primarily directed to forming an array of nanopores. However, it will be appreciated that the same approach can be used to form a single nanopore.

30 [0018] In accordance with the present invention, a technique is provided for forming an array of molecules aligned in a pre-selected defined orientation relative to

the substrate. In one embodiment, that orientation is preferably substantially perpendicular. The array of molecules is formed by dispersing them in an array of small, aligned holes (nanopores) in a substrate. Typically, the material in which the pores are formed is electrically insulating. The underlying substrate may be either electrically  
 5 conducting or insulating. For electronic device applications, the substrate is generally electrically conducting and may be exposed and accessible at the bottom of the pores so that one end of the molecule in the nanopore makes electrical contact to the substrate. A substrate such as a single-crystal silicon wafer is especially convenient because many of the process steps to form the molecular array can use techniques al-  
 10 ready well developed for integrated-circuit fabrication. For example, heavily doped silicon has sufficient electrical conductivity to serve as one electrode for the molecules. Alternatively, a metal layer can be formed over the silicon or over an oxide on silicon if lower resistivity or electrical isolation is needed.

**[0019]** The following steps are used to form the array:

**[0020]** Turning to FIG. 1a, a substrate 10 is shown. The substrate, if insulat-  
 15 ing, may be an oxide, such as silicon dioxide or aluminum oxide, or a nitride, such as silicon nitride, or an oxynitride, such as silicon oxynitride, or a carbide, such as silicon carbide. If conducting, the substrate may be heavily doped single crystalline or poly-  
 crystalline silicon or a metal or a metal layer over silicon or silicon dioxide.

**[0021]** Next, an etch mask of nanoscopic dimensions is applied to the sub-  
 20 strate 10, for example, using nanoparticles 12. Nanoparticles of well controlled dimensions are readily available. For example, suspensions containing nanoparticles may be commercially obtained. One such source, Ted Pella, Inc. (Redding, CA), provides gold nanoparticles in a sol, with gold particles available in specific sizes ranging  
 25 from about 2 nm to 250 nm. These nanoparticles are usually composed of an inorganic crystalline core, typically a metal, that is coated with an organic species to keep the nanoparticles from agglomerating. These nanoparticles 12 can be dispersed on the sur-  
 face 10a of the substrate 10 from the liquid phase. Alternatively, the nanoparticles 12 can be formed by depositing a material of one lattice constant on a substrate having a  
 30 different lattice constant and using the forces from the lattice mismatch to form nano-  
 particulate islands of the depositing material. As shown in FIG. 1a, the nanoparticles

12 are distributed on a major surface 10a of the substrate 10 to a coverage less than a single layer. That is, the nanoparticles are separated from each other by a space and there are no multiple layers of the nanoparticles.

5 [0022] In either case, the nanoparticles 12 are then used as an etch mask, and the substrate 10 is directionally etched, for example using reactive ion etching (RIE) to a controlled depth. The etch chemistry and nanoparticulate material 12 are selected so that the material comprising the substrate 10 is etched much faster than the nanoparticulate material. This etch process produces an array of pillars 110 on the new surface 10a' of the substrate 10. The nanoparticulates 12 may be removed before further  
10 processing or may be left on the pillars 110 (and typically removed during subsequent processing). As shown in FIG. 1b, the nanoparticles 12 serve as an etch mask for directional RIE, leaving pillars 110 on an etched surface 12b.

[0023] Because the nanoparticles 12 comprise a metallic core, they are better able to withstand the rigors of RIE, and are not readily ablated, as are organic polymers. The ability to survive longer during RIE means that taller pillars, and hence  
15 deeper nanopores, can be fabricated.

[0024] It will be appreciated that the cross-section of a pillar need not be perfectly uniform over its entire height, but may evidence some taper, as a consequence of the etching process.

20 [0025] The length of the pillars 110 can be tailored to have a specific relation to the length of the molecules to be inserted in the formed nanopores. The remaining thickness of the substrate 10 (the distance between back surface 10b and the new front surface 10a') must be sufficient to provide suitable mechanical strength to the substrate 10.

25 [0026] Next, the array of pillars 110 must be transformed into a corresponding array of holes 16, in which the molecules 18 can be placed. This is accomplished in the following manner: An insulating material 14 is formed on the surface 10a' of the substrate 10, surrounding and covering the pillars 110. Examples of suitable insulating materials include oxides, such as silicon dioxide and aluminum oxide, nitrides, such  
30 as silicon nitride, oxynitrides, such as silicon oxynitride, carbides, such as silicon carbide, and diamond-like carbon (DLC). Silicon dioxide may be formed by any number

of well known techniques, including, but not limited to, thermal deposition and spin-on-glass (SOG). Thin aluminum oxide, for example, on the order of 12 to 25 Å thick, is formed by totally reacting aluminum in oxygen during deposition or depositing Al and oxidizing afterwards. Still further examples of suitable insulating materials include polymers that have the requisite chemical and electrical properties, i.e., a slower differential etch rate than the pillars 110 and electrically insulating attributes. Such insulating polymers are well known; an example includes polyfluoroalkylenes, which may be produced in a carbon-hydrogen-fluorine plasma.

**[0027]** The insulating material 14 may be formed by chemical vapor deposition or by liquid-phase techniques commonly used in semiconductor device processing. Good filling of the space between the pillars 110 is critical. The surrounding material 14 will typically extend above the top of the pillars 110 so that the pillars are completely covered, but this is not essential. Depending on the subsequent processing, a resultant flat (planar) top surface 14a may or may not be important. As shown in FIG. 1c, a layer 14 of an oxide, e.g., silicon dioxide ( $\text{SiO}_2$ ), is blanket-deposited, employing well-known deposition techniques, to completely or partially cover the pillars 110. Examples of suitable deposition methods include chemical vapor deposition (CVD) (e.g., high density plasma CVD or thermal CVD or ozone-assisted CVD or plasma-enhanced CVD) and spin-coating, all of which are well-known in the art of semiconductor device fabrication.

**[0028]** If the pillars 110 are not already exposed, the insulating material 14 surrounding and covering the pillars is then reduced in thickness so that the tops 110a of the pillars are exposed. This material removal may be accomplished by chemical-mechanical polishing (CMP), a technique commonly used in integrated-circuit fabrication. In this case, having a flat top surface 14a before polishing is not critical. At the end of this step, the surface 14a' is flat; the surface is composed of both the exposed ends of the pillars 110a and the surrounding insulating material 14. FIG. 1d shows the resulting structure after polishing, leaving a flat surface 14a' in the insulating layer 14.

**[0029]** Alternatively, the material removal may be accomplished by an unmasked single- or multi-step plasma/reactive-ion etch technique. In this case, the top surface 14a must be flat before the start of the etch process. The selectivity of the

plasma/reactive-ion etch can be adjusted during different portions of the etch process to produce either a flat surface 14a' (same etch rate) or a surface with the ends 110a of the pillars 110 either recessed or protruding (different etch rates), as desired. Both CMP and plasma/reactive-ion etching are processes well known in integrated-circuit processing.

**[0030]** If the layer 14 is deposited in such a manner as to form thinner regions over the pillars 110, then the un-masked etch step above does not require that the top surface 14a be flat, as the etching will expose the top of the pillar 110 before the surrounding area is exposed.

**[0031]** As the final step, the pillars 110 are removed, leaving nanopores 16 extending a specified distance into (or beyond) the insulating material 14, by employing a selective etch. Because of their extremely small size, the pillars 110 are best removed by gas-phase etching. For example, a selective chemical or plasma etch can remove the pillar material 110 without significantly attacking the surrounding insulating material 14. If a plasma is used, its composition is selected to be chemically selective, rather than relying on high-energy/high-density ion bombardment. FIG. 1e shows the resulting structure, after etching away the pillars 110, leaving nanopores 16 where the pillars were originally located.

**[0032]** The nanopores 16 are intended, at least in some applications, to be approximately the size of molecules that are to be placed in them. For example, many long-chain molecules are about 10 nm long and about 1 nm in diameter. The size (diameter) of the nanopores 16, of course, depends on the size of the pillars 110. Broadly, however, the nanopores 16 may be formed having a length within the range of about 5 to 100 nm and a diameter within the range of about 1 to 10 nm. It is expected that the aspect ratio (length:diameter) is likely to be less than about 100:1 and, for practical considerations, less than about 25:1.

**[0033]** At this point, the array of nanopores 16 is essentially complete. The molecules 18 can then be dispersed over the surface. Many of the molecules fill the nanopores 16 and become aligned preferentially in the direction of the nanopores. The degree of alignment depends on the relative diameters and lengths of the nanopores 16

and molecules 18. FIG. 1f illustrates the filling of the nanopores 16 with molecules or other material 18.

[0034] By proper processing techniques before applying the molecules 18, the bottom of the nanopores 16 may be made electrically conducting, either by separate deposition of an electrically-conducting film as a buried layer in the substrate 10 or by use of an electrically conductive substrate 10. Alternatively, the bottom of the nanopores 16 may be covered by a thin tunnel barrier so that a controlled electrical connection between the molecules and the underlying substrate can be made for advantageous use of the molecules in an electronic device. In other cases, a thick insulator may remain if the molecule needs to be electrically isolated.

[0035] The array of nanopores 16 that is formed can find a variety of uses. For example, it may be desirable to characterize a molecule. Such nanopores 16 can isolate individual molecules from each other and permit probing, such as by scanning tunneling microscopy (STM). Alternatively, it may be desirable to form molecular electronic devices. The nanopores 16 not only isolate, or separate, the individual molecules from each other, but, in the case of long-chain molecules, prevent bending or kinking of the molecules.

[0036] Molecular electronic devices may employ molecules that are capable of switching in the presence of an electric field. Examples of such molecules include the rotaxanes, pseudo-rotaxanes, catenanes, and spiropyrans. For such devices, the substrate 10 forms one electrode, and it is easily within the ability of one skilled in this art, based on the teachings that are emerging, to form a suitable second electrode for applying the electric field.

[0037] Filling the nanopores 16 with a material 18 such as a semiconductor or a magnetic material can be used to produce electronic or magnetic devices. The nanopores can be filled by a selective chemical vapor deposition process or possibly by electrochemical deposition. In either case, the nanopore is filled from the bottom toward the top. More conventional processes that nucleate material on the walls of the pore will be difficult to implement because of the small diameter and high aspect ratio of the nanopores 16.

[0038] The foregoing discussion is directed primarily to the preferred orientation of the nanopores 16 relative to the substrate 10, namely, substantially perpendicular. Other orientations may also be obtained, less than 90 degrees, such as by changing the angle of the etch source to the substrate or tilting the substrate during directional etching.

### INDUSTRIAL APPLICABILITY

[0039] The method of forming a nanopore array is expected to find use in the fabrication of molecular electronic devices and for the physical and electrical characterization of molecules.